

Notice of References Cited	Application/Control No. 10/015,899		Applicant(s)/Patent Under Reexamination WATANABE ET AL.	
	Examiner SATISH RAMPURIA		Art Unit 2191	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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*	B	US-5,831,868 A	11-1998	Beausang et al.	716/18
*	C	US-5,903,466 A	05-1999	Beausang et al.	716/18
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	K	US-			
	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Kao et al., Automatic generation of load board schematics for testing mixed signal ICs; 1993, IEEE, Pages: 1-6
	V	Kusiak et al., Design of modular digital circuits for testability; 1997, IEEE, Vol. 20, Issue 1, Pages: 48-57
	W	Beenker et al., Macro Testing: Unifying IC And Board Test; 1986, IEEE, Vol. 3, Issue 6, Pages: 26-32
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.